October 10, 2001

INFORMATION DISCLOSURE STATEMENT letter

To Whom It May Concern:

The following documents are included in form PTO/SB/08A Information Disclosure Statement by Applicant as a bibliography for the application having the following title and applicant.

Title: Shared Multiplication in Signal Processing Transforms

Applicant: Charles D. Murphy

Here, the documents are discussed as they relate to the specification and claims of the application.

The present invention proposes multipliers that share calculations. These multipliers are used in computing sums of products. Many signal processing transforms compute sums of products. Some useful features of such signal processing transforms are that they may have fixed, known weights and that each transform input may appear in several different sums or outputs. While there may be special mathematical relations between the number values of numbers being multiplied, there may also be special properties of finite-precision numeric formats or of representations of the number values. The present invention exploits these features. The goal of sharing calculations is to reduce the overall cost of computing the sums of products.

Prior art multiplication techniques have concentrated on design trade-offs between general use and implementation cost. A general multiplier is one which can accept two numbers and compute their product. The two numbers may take on any values allowed by their finite-precision numeric formats. A general multiplier is very flexible. It can be re-used without any changes in computing many different products. However, a general multiplier is relatively expensive, since it must be able to deal with any input values permitted by the input numeric formats.

There are many types of general multipliers used in digital computation. Details of general multiplier designs are beyond the scope of this IDS letter. However, a basic discussion of general multiplication is available in any textbook on computer engineering or introductory digital logic.

For signal processing transforms such as the discrete Fourier transform, the inverse discrete Fourier transform, and the discrete cosine transform, which compute sums of weighted inputs, the weights are known constants. Constant multipliers have been proposed as replacements for general multipliers when using circuits or software dedicated to the computation of these transforms. A constant multiplier can multiply a first number by a constant. The first number can take on any value allowed by its finite-precision numeric format. A constant multiplier can have much lower cost than a general multiplier if properties of the constant's number value, finite-precision numeric format, or representation are exploited.

Several US patents are cited as prior art examples of constant multipliers or constant multiplier design techniques in the present application. These include US Patent

6,223,197 (issued to K. Kosugi on April 24, 2001), US Patent 5,903,470 (issued to A. Miyoshi and T. Nishiyama on May 11, 1999), US Patent 5,841,684 (issued to K. Dockser on November 24, 1998), US Patent 5,815,422 (issued to K. Dockser on September 29, 1998), US Patent 5,600,569 (issued to T. Nishiyama and S. Tsubata on February 4, 1997) and US Patent 5,159,567 (issued to J. Gobert on October 27, 1992).

US Patent 6,223,197 issued to K. Kosugi on April 24, 2001 entitled "Constant multiplier, method and device for automatically providing constant multiplier and storage medium storing constant multiplier automatic providing program" discusses the notion of multiplication of two numbers in a signal processing transform when one of the numbers is a transform weight that is known and fixed. It also discusses some techniques for multiplying two numbers together, particularly with finite-precision numeric formats based on power-of-two representations using binary representation elements.

The claims of US Patent 6,223,197 all relate to a single constant multiplier or to methods for designing a single constant multiplier. The claims and specification do not consider the possibility of multipliers that share calculations.

US Patent 5,903,470 issued to A. Miyoshi and T. Nishiyama on May 11, 1999 entitled "Method and apparatus for automatically designing logic circuit, and multiplier" covers methods and apparatus for generating constant multiplier circuits. Again, the claims and specification do not consider the possibility of multipliers that share calculations, either constant multipliers or non-constant multipliers.

US Patent 5,841,684 issued to K. Dockser on November 24, 1998, entitled "Method and apparatus for computer implemented constant multiplication with multipliers having repeated patterns including shifting of replicas and patterns having at least two digit positions with non-zero values" and US Patent 5,815,422 issued to K. Dockser on September 29, 1998 entitled "Computer-implemented multiplication with shifting of pattern-product partials" both relate to constant multiplication.

In particular, these two patents discuss reducing the cost of a multiplication by computing a partial product and shifting the partial product to duplicate the contribution of another partial product. The reduction comes if the shifting operation has lower cost than computation of the other partial product. From the perspective of the present invention, these prior art techniques involve a constant multiplier which computes intermediate terms and then shares them with itself in computing a single desired product. In contrast, the present invention proposes sharing calculation between multipliers that compute different products, or sharing for different product computations in a single multiplier that computes more than one product.

Another prior art example of shared computation within a single multiplier appears in US Patent 4,868,778 issued to J.E. Disbrow on September 19, 1989 entitled "Speed enhancement for multipliers using minimal path algorithm". This patent also discusses cost reduction techniques for twos complement representations based on choosing whether multiplication or the combined steps of negation, multiplication by the negated value, and negation have lower cost. US Patent 5,159,567 issued to J. Gobert on October 27, 1992 entitled "Programmable serial multiplier" discusses similar cost reduction techniques.

US Patent 5,600,569 issued to T. Nishiyama and S. Tsubata on February 4, 1997 entitled "Method, system, and apparatus for automatically designing logic circuit, and multiplier" covers the design of constant multiplier circuits. It has 44 claims for circuit design procedures, and an extensive discussion of how to automate methods for producing low-cost multipliers. However, it does not consider multipliers for different products which share calculations.

In addition to the constant multipliers above, there are a variety of prior art constant multipliers that exploit properties of particular number values and of particular finite-precision numeric formats. Examples which appear in the present application are addition of a number to itself to implement multiplication by 2, shifting of binary representations to implement multiplication by powers of two, and negation and shifting to implement complex multiplication by weights of a four-point discrete Fourier transform. These prior art examples of low-cost multiplication have been used in computing discrete Fourier transforms and in computing inverse discrete Fourier transforms.

The patent application "Non-Constant Reduced-Complexity Multiplication in Signal Processing Transforms" with application number 09/963623 and filing date September 27, 2001, by the inventor of the present invention proposed multipliers which are not constant multipliers and which are not general multipliers. These non-constant, non-general multipliers have greater flexibility than constant multipliers and lower cost than general multipliers. They exploit restrictions on the allowed values of one or both numbers being multiplied.

The present invention can be applied to constant multipliers, to general multipliers, or to the non-constant, non-general multipliers of "Non-Constant Reduced-Complexity Multiplication in Signal Processing Transforms". Originally, the present invention was conceived in conjunction with the invention of "Non-Constant Reduced-Complexity Multiplication in Signal Processing Transforms". However, that application turned out to have 32 claims on its own, and the inventor decided to submit the present invention in a separate application.

Another example of prior art cited in the present application appears in US Patent 4,354,249 issued to T.M. King and S.M. Daniel on October 12, 1982 entitled "Processing unit for multiplying two mathematical quantities including at least one complex multiplier". The prior art invention is a complex multiplier that can compute the product of a first complex number and a second number, or the product of the first complex number and the complex conjugate of the second complex number. The prior art invention has a switch for determining which product is computed.

In the application of the present invention it was pointed out that the invention of US Patent 4,354,249 could be modified to produce both products without re-computing the results used in the final combining stage. One way would be to include separate final combining stages for each product. Another way would be to compute and store one product, then switch the control in the invention of US Patent 4,354,249 to provide the other product. Such modifications would result in complex multiplication using shared computation.

One explicit difference between the modification of the invention of US Patent 4,354,249 suggested in the present application and the invention of the present application is that most of the claims of the present invention cover multiplication of real numbers. The

present invention could be applied to the real number multipliers in the modified invention depending on the number values and representations of the real components of the complex numbers being multiplied. This could lead to even lower cost for computing the two products. Claims in the present application that do not specify real number multiplication require that the products not be of a first number and both a second number and the complex conjugate of the second number. Complex numbers that do not have the special property of being complex conjugates can have representations to which the present invention can be applied.

The present application discusses very briefly fast Fourier transform (FFT) techniques. A full discussion of FFT techniques is beyond the scope of both the present application and this IDS letter. Further material on FFT techniques is available in most textbooks on digital signal processing and in a large number of technical papers. The present application points out that the decomposition which enables FFT techniques to reduce the complexity of computing a discrete Fourier transform of size N from $O(N^2)$ to O(N log N) results in implicit sharing of calculations used in computing the contribution of each transform input to each transform output.

The reduced complexity of FFT techniques depends entirely on special properties of the number values of discrete Fourier transform weights. The present invention, in contrast, can exploit properties of representations of these weights in particular finite-precision numeric formats. The present invention can be applied in addition to FFT techniques. Also, the present invention can be applied to transforms that do not have the convenient mathematical relations between discrete Fourier transform weights.

Thus far, discussion of prior art has focused on constant multipliers and multiplication methods, on non-constant, non-general multipliers and multiplication methods, and on techniques for fast computation of discrete Fourier transforms. Constant and non-constant, non-general multiplication techniques can reduce the cost of computing a signal processing transform by exploiting restrictions on multiplied numbers to obtain a low-cost multiplier implementation. Fast Fourier transform techniques can reduce the cost of computing a signal processing transform by reducing multiplication count via implicit shared computation.

"Low cost" can refer to financial cost, small size, low power consumption, or some other measure. Cost reductions that take into account features of a signal processing transform are important in the design of improved signal processing systems.

I, the inventor of the present invention have been unable to find any prior art closely similar to the material of the present invention. To the best of my knowledge, the idea of sharing calculation results between two or more product computations when computing sums of products is new and deserving of patent protection.

This concludes this INFORMATION DISCLOSURE STATEMENT letter.

Sincerely,

Charles D. Murphy

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Charles D. Murphy
Group Art Unit	
Examiner Name	
Attorney Docket Number	

09/976920
10/15/01

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6223197		K. Kosugi	04 24 2001	
		5903270		A. Miyoshi + T. Nishiyama	05 11 1999	
		5841684		K. Dockser	11 24 1998	
		5815422		K. Dockser	09 29 1998	
		5600569		T. Nishiyama + S. Tsubata	02 04 1997	
		5159567		J. Gobert	10 27 1992	
		4868778		J. Dishrow	09 19 1989	
		09/963623		C.D. Murphy	09 27 2001	
		4354249		T.M. King + S.M. Daniel	10 12 1982	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.